

FIG. 1

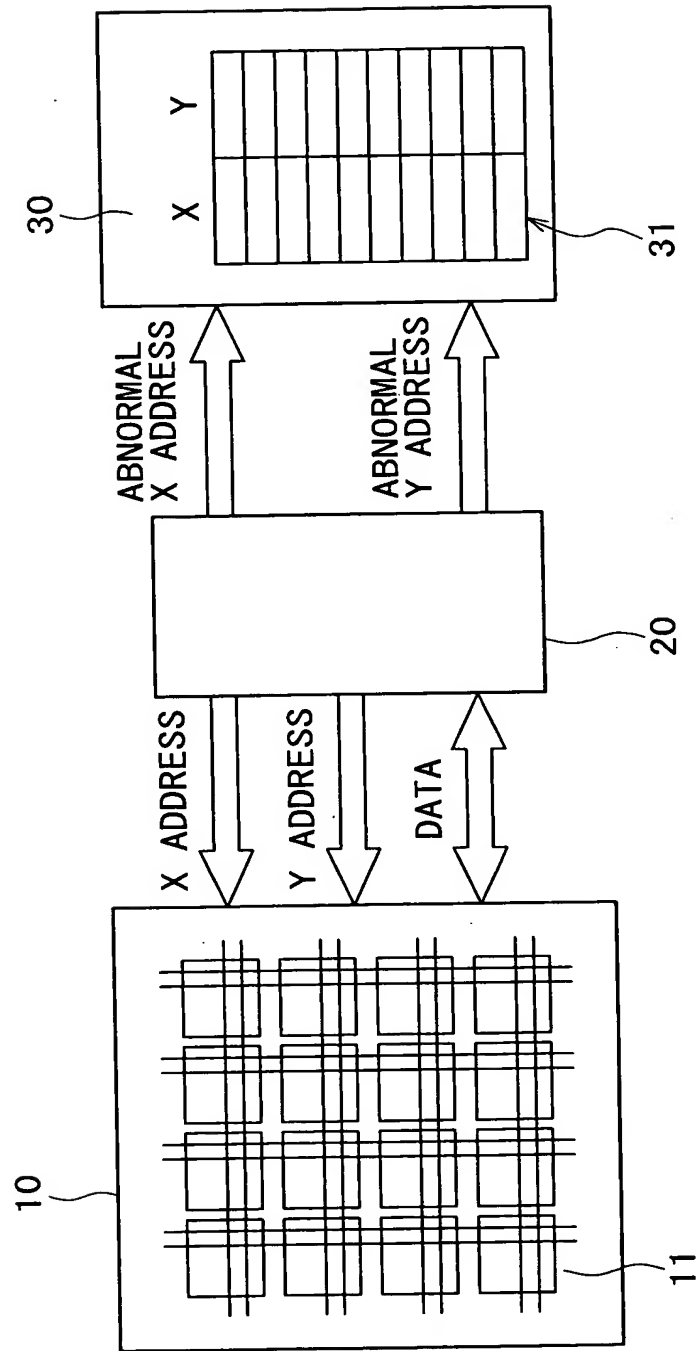


FIG. 2

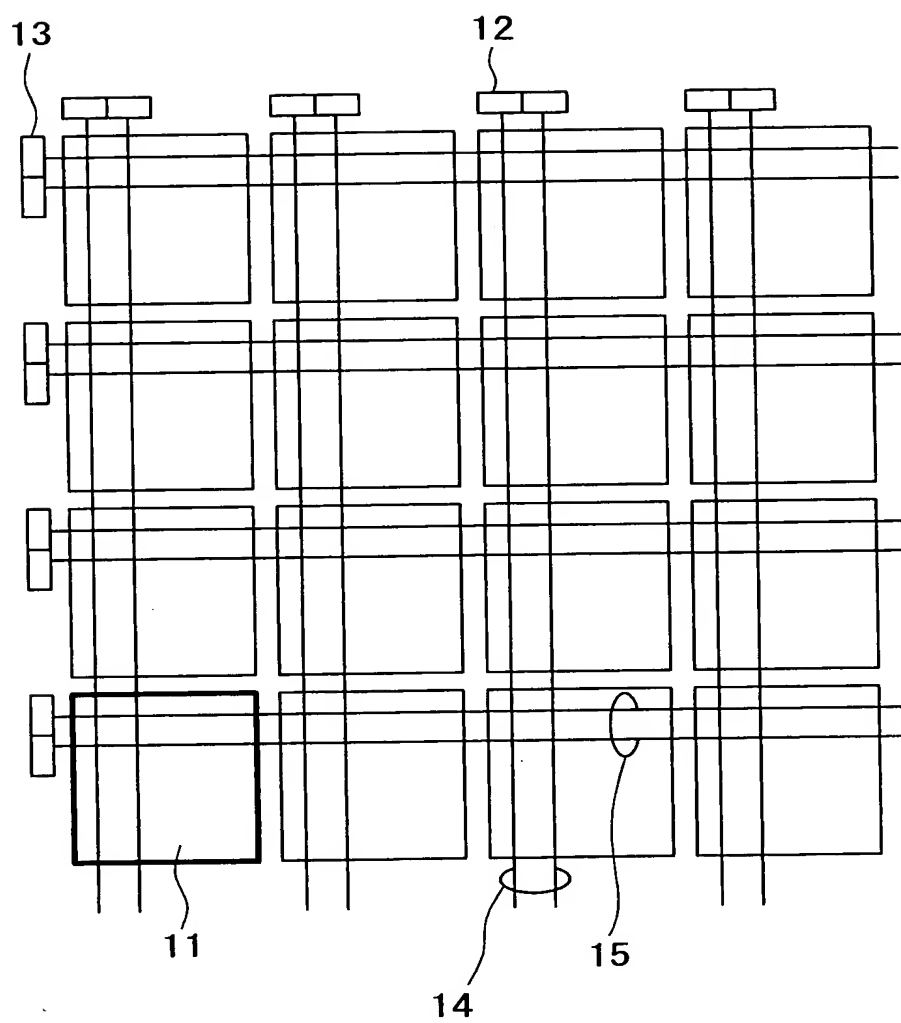


FIG. 3

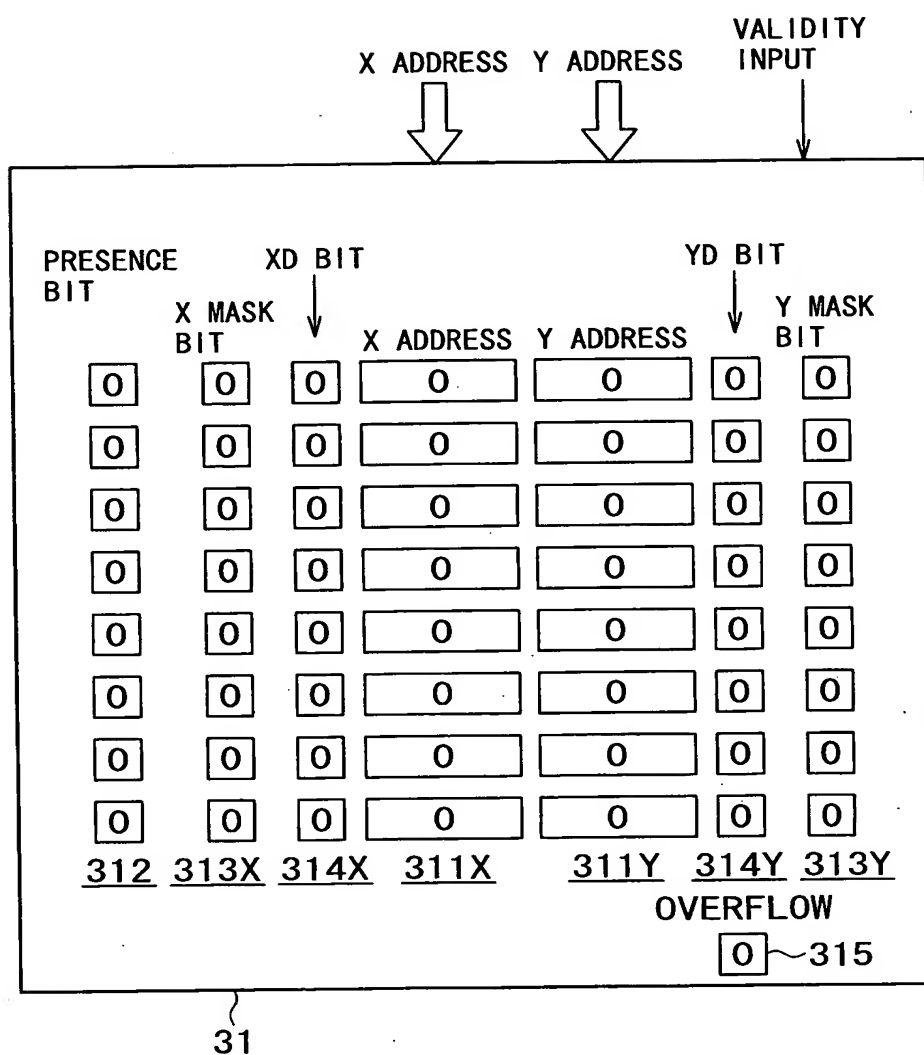


FIG. 4

PRESENCE BIT	X MASK BIT	XD BIT ↓	X ADDRESS	Y ADDRESS	YD BIT ↓	Y MASK BIT
1	0	0	12	5	0	0
1	0	0	6	5	1	1
1	1	1	12	8	0	0
1	0	0	5	35	0	0
1	0	1	6	35	1	0

OVERFLOW  
0

F I G. 5

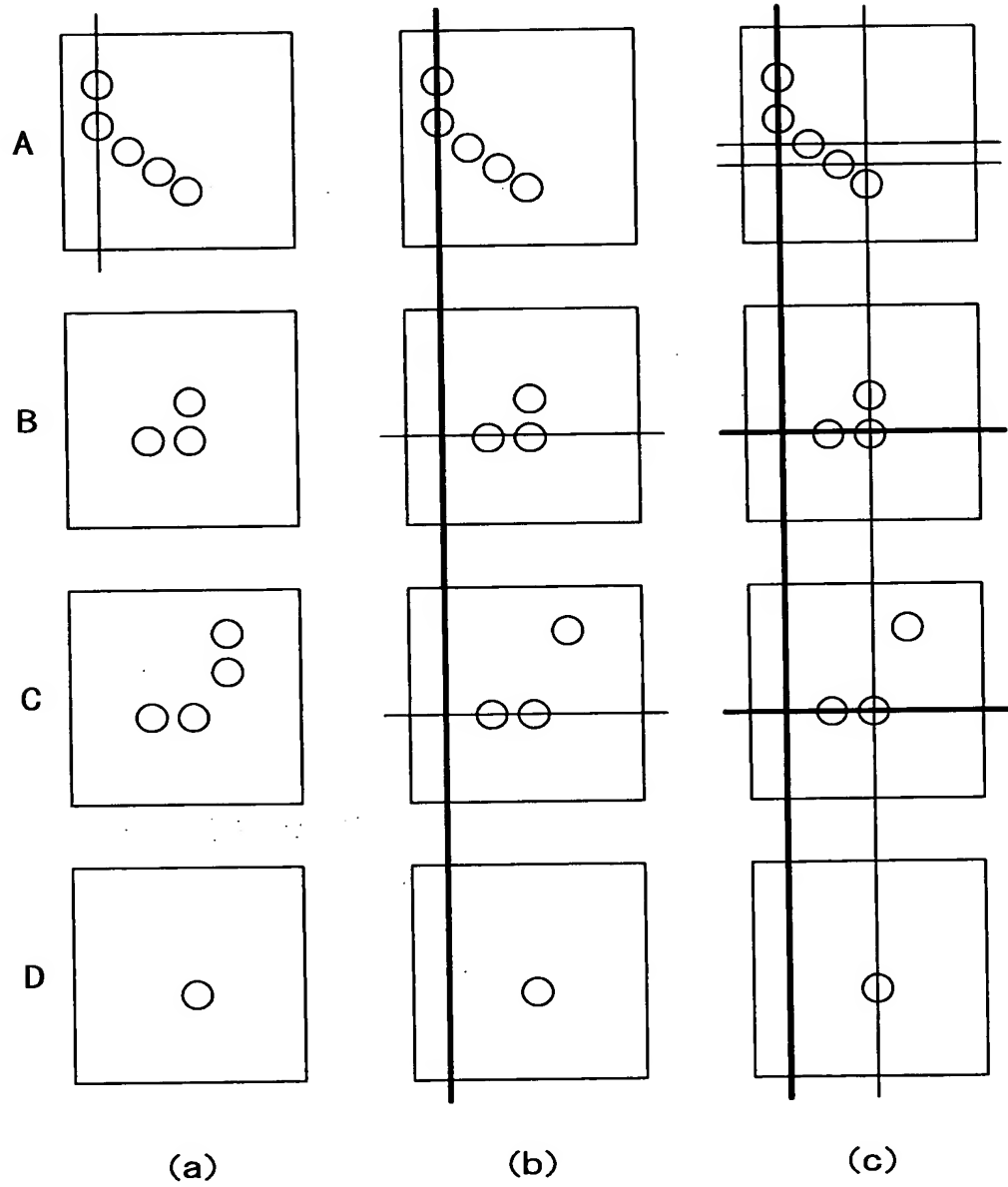


FIG. 6

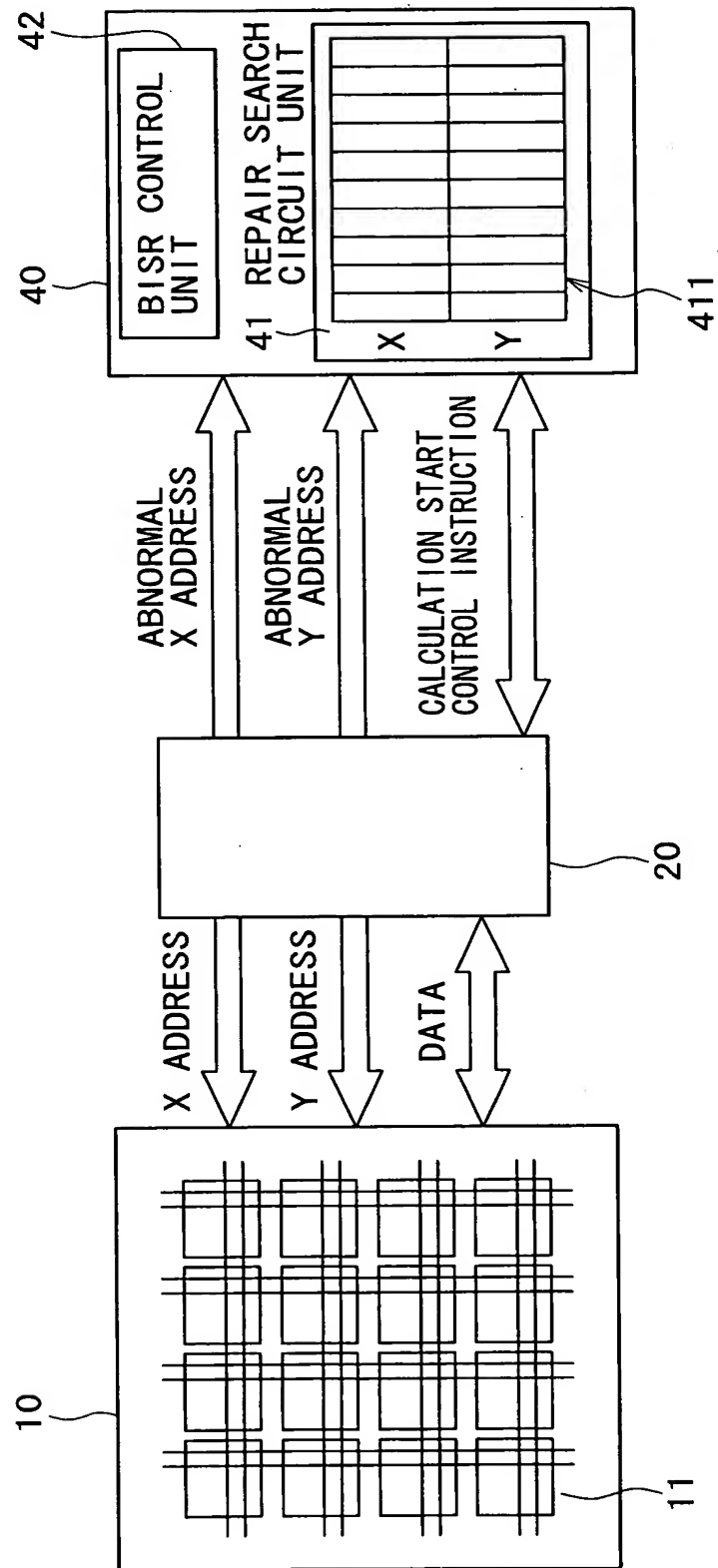


FIG. 7

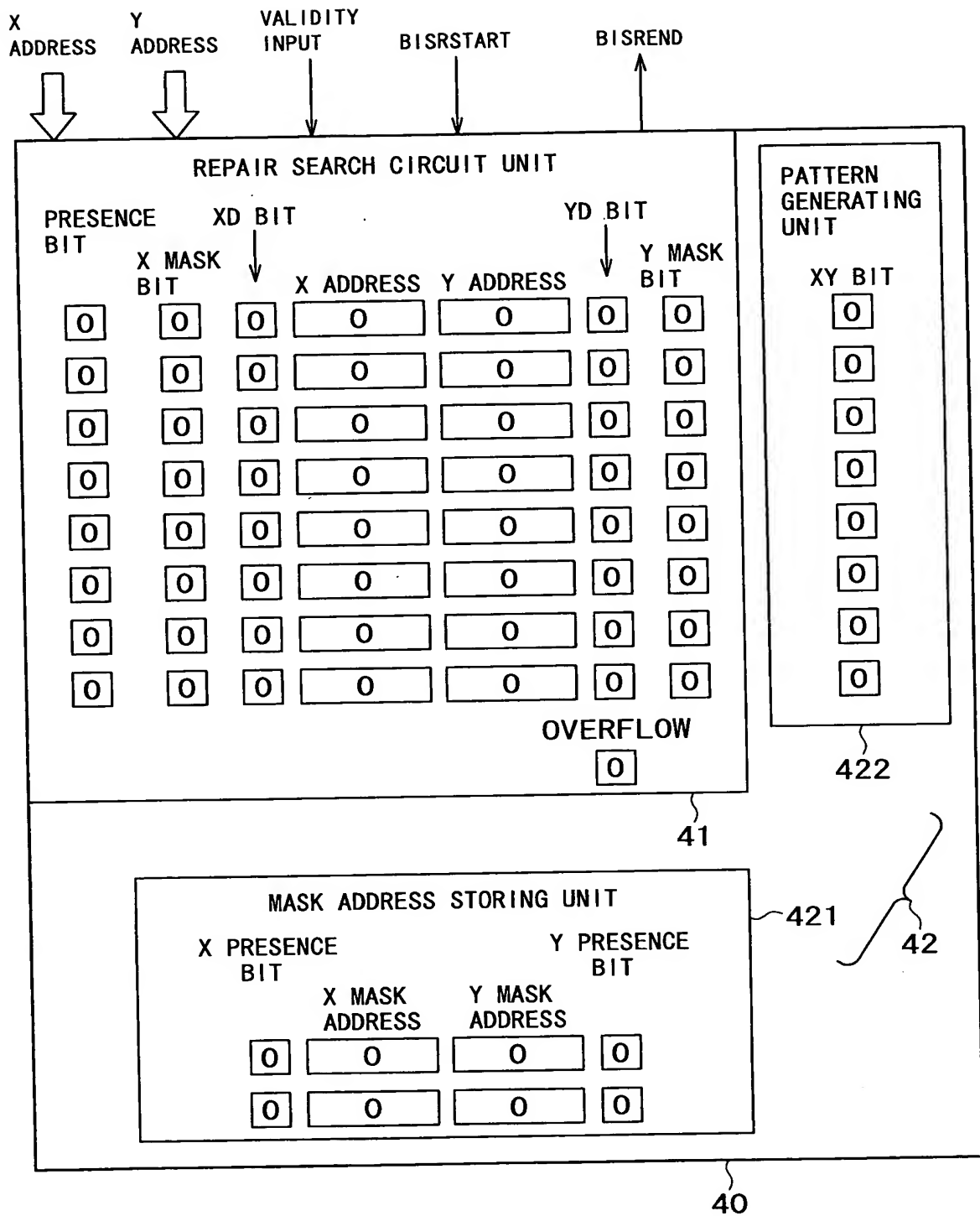


FIG. 8

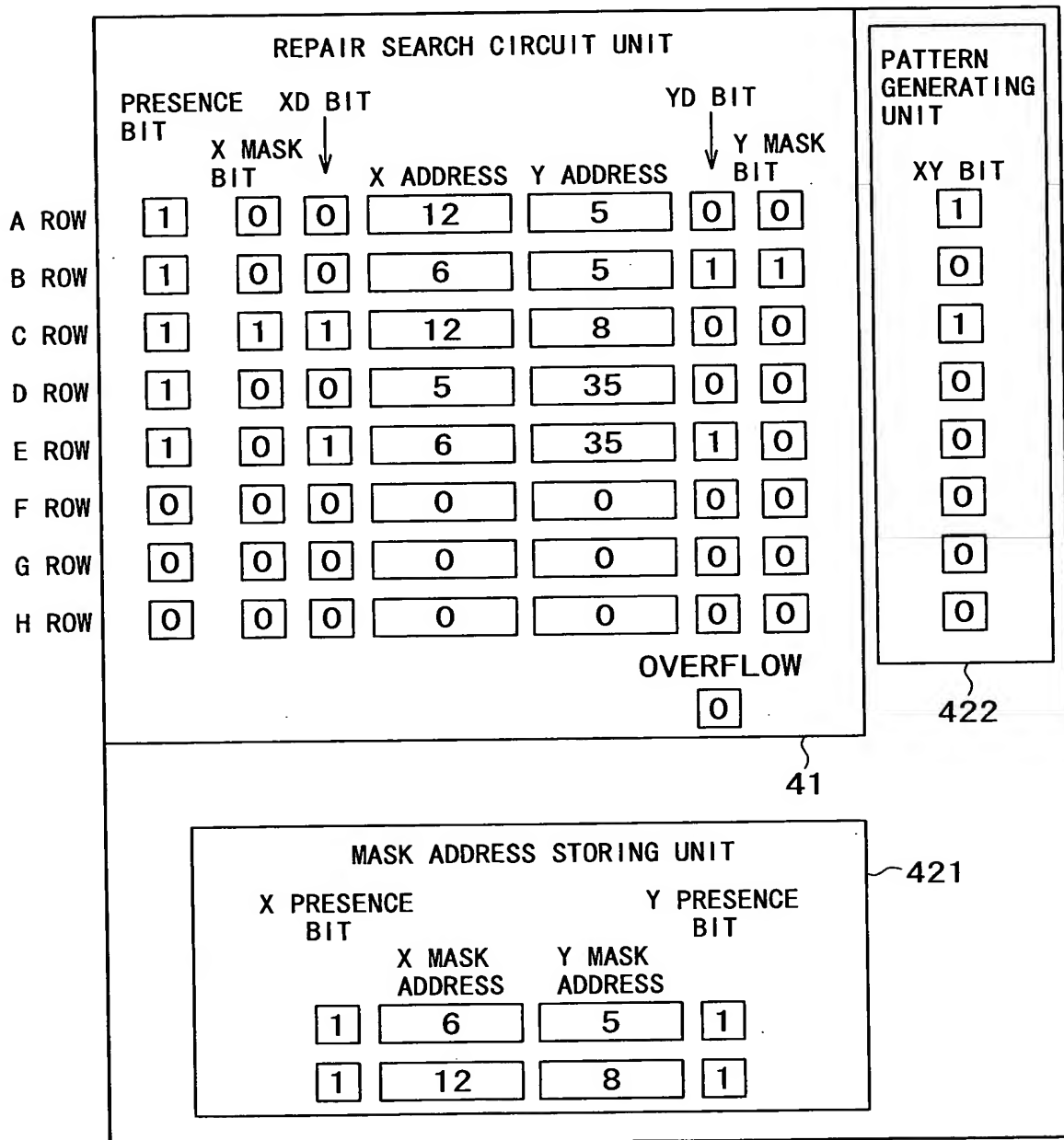




FIG. 9

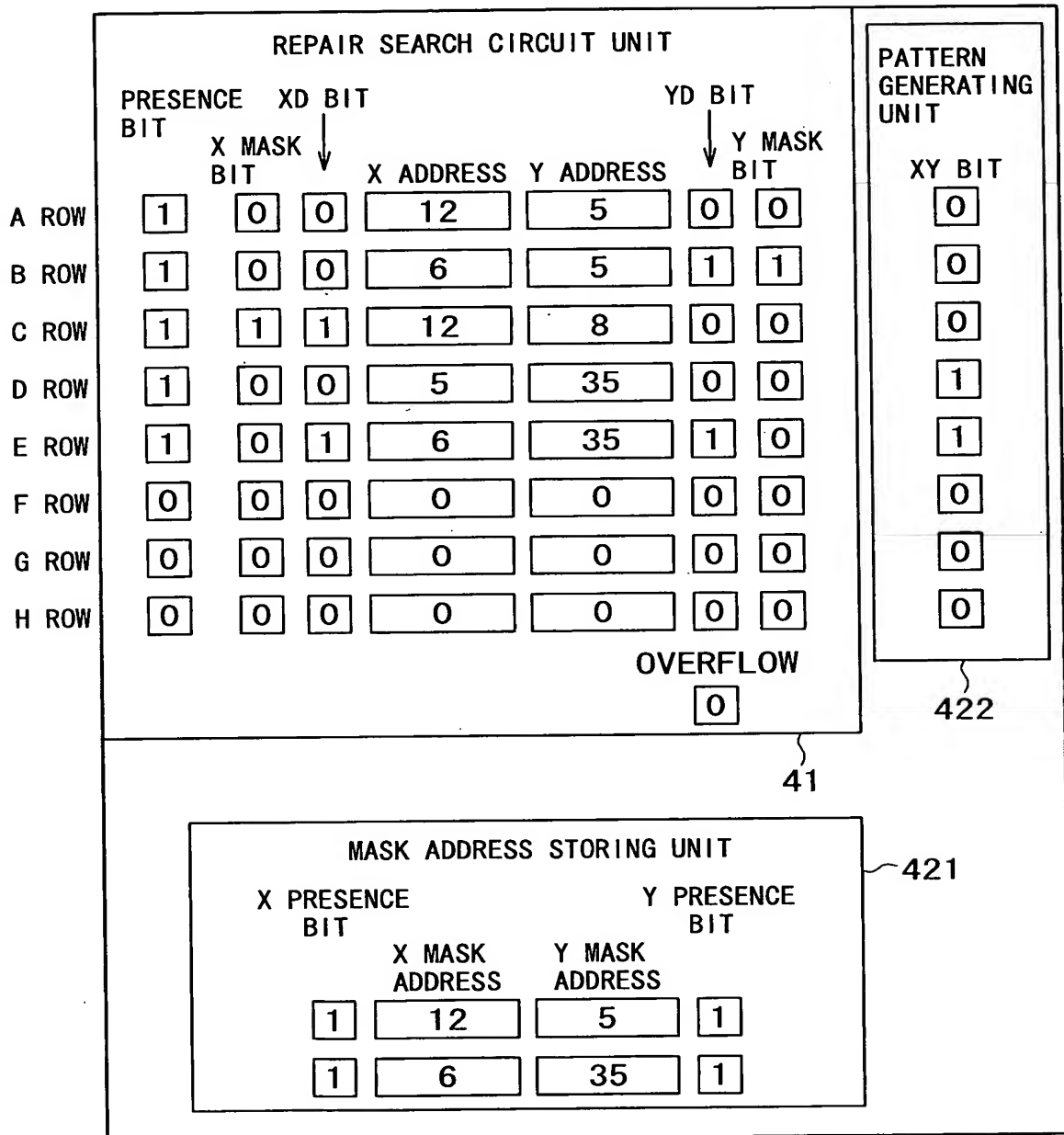


FIG. 10

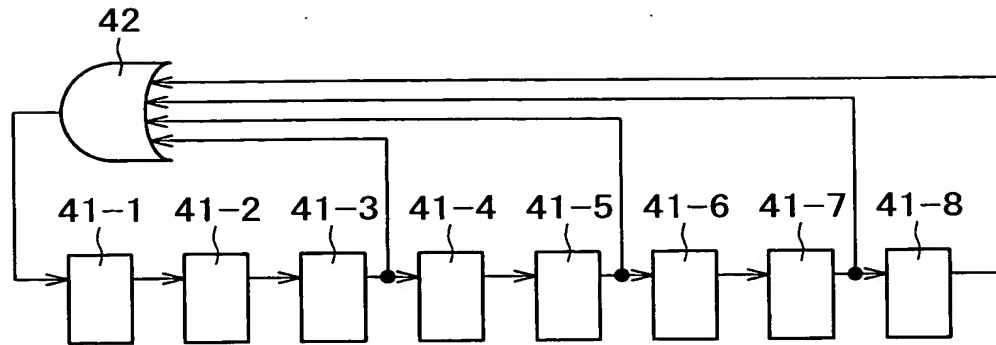


FIG. 11A

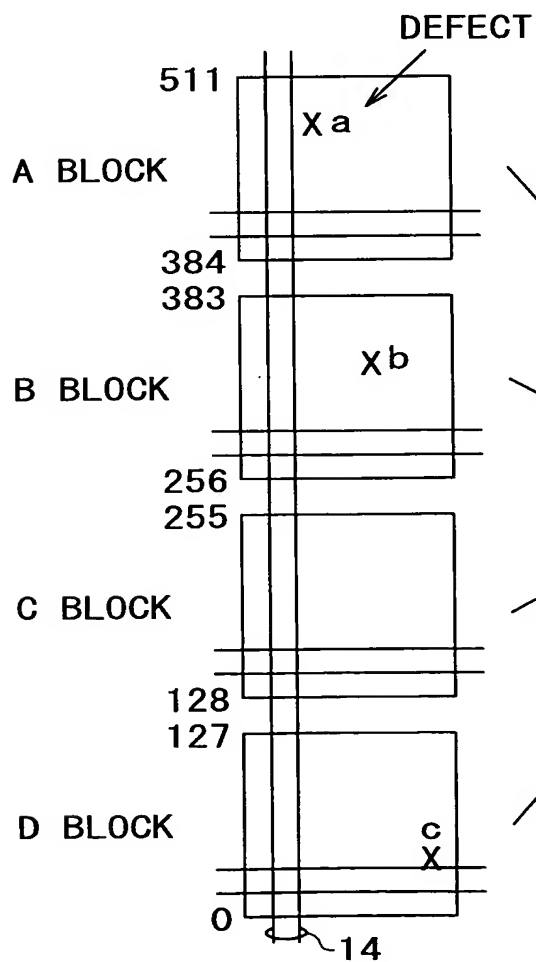


FIG. 11B

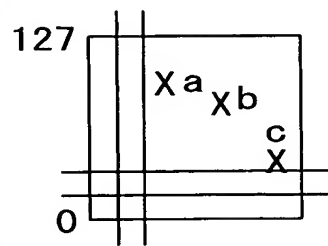


FIG. 12A

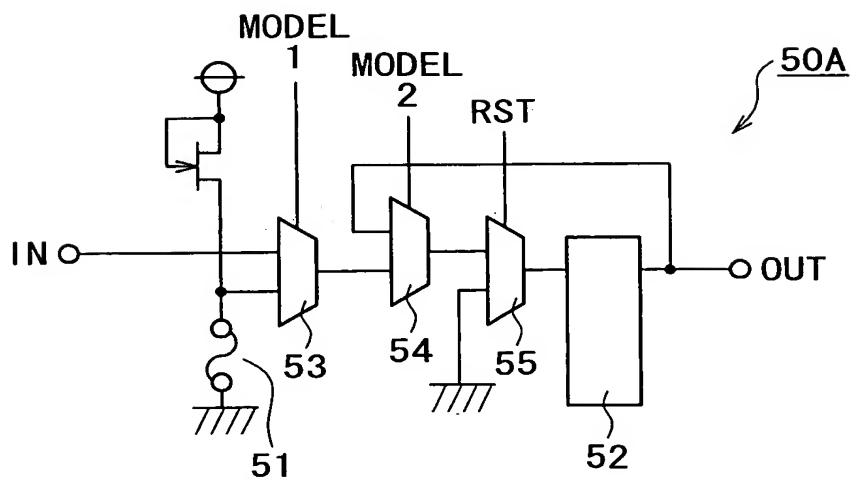


FIG. 12B

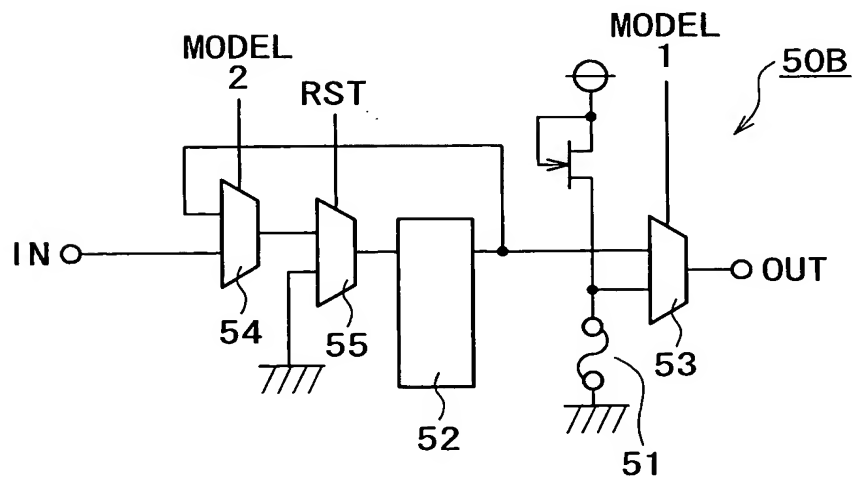


FIG. 13

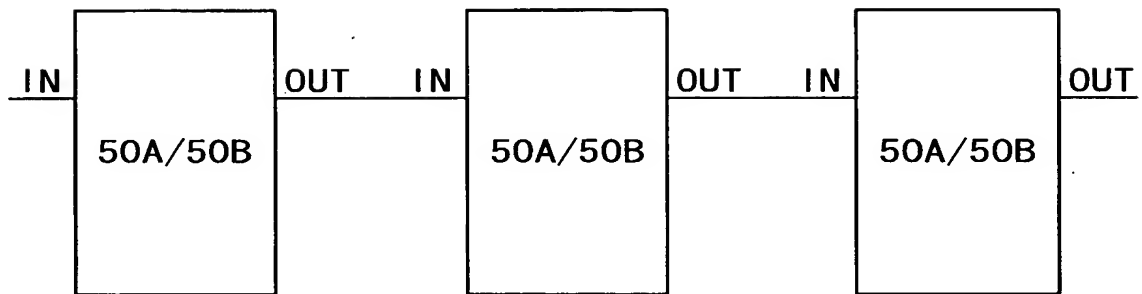


FIG. 14

